REMARKS/ARGUMENTS

The Office Action mailed April 26, 2004, has been received and reviewed. Claims 1 through 23 are currently pending in the application. Claims 1 through 22 stand rejected. Claim 23 has been added as a new claim. Applicant has amended claims 1-3, 6, 8-13, 15 and 19-22, and respectfully requests reconsideration of the application as amended herein.

A substitute specification has been submitted and is herewith attached. The substitute specification includes minor modifications described below, as requested by the Examiner. In addition to the modifications described below, the substitute specification includes paragraph numbering and changes pursuant to the previously submitted preliminary amendment of June 29, 2000.

In the specification, paragraph [0003] has been amended to clarify the description. The date parenthetical of the Ishii patent has been modified. "Sep" has been replaced with "issued September."

In the specification, paragraph [0004] has been amended to clarify the description. The date parenthetical of the Gagnon patent has been modified. "Jul" has been replaced with "issued July."

In the specification, paragraph [0006] has been amended to clarify the description. The date parenthetical of the Yamamoto patent has been modified. "Sep" has been replaced with "issued September." The date parenthetical of the Kametani patent has been modified. "Dec" has been replaced with "issued December." The date parenthetical of the Yamamoto patent has been modified. "Dec" has been replaced with "issued December." The date parenthetical of the Millar patent has been modified. "Aug" has been replaced with "issued August."

In the specification, the title "Brief Description of the Several Views of the Drawings" has been replaced with "Brief Description of the Drawings."

In the specification, paragraph [0028] has been amended to clarify the description of Figure 4. The phrase "between the upper surface of the substrate 12 and the upper surface of the

circuit trace 14," has been inserted after the phrase "and the height ("H")" to both clarify the term "H" and define substrate 12 as shown in Figure 4.

In the specification, paragraph [0031] has been amended to clarify the description of Figure 8. On the first line of the paragraph, the term "substrates" has been replaced with the term "substrate," because Figure 8 only depicts one substrate. The term "adjacent" has been inserted into the third line of the paragraph to clarify the phrase that now reads "placed between two adjacent signal traces." The reference numeral "21" has been added on the sixth line of the paragraph after the term "second surface" to conform with the labeling of Figure 8.

In the specification, paragraph [0034] has been amended to clarify the description of Figure 13. On line four of the paragraph, after the term "gap 40," the parenthetical "(see Figure 13)" has been inserted to properly reference the reference numeral "40." Also, on the twentieth line of the paragraph, after the term "passivation layer," the reference numeral "50" has been inserted, followed by the phrase "(see Figures 8, 12 and 13)," in order to adequately explain the corresponding modifications to the figures.

In the specification, paragraph [0035] has been amended to clarify the description of Figure 14. The acronym "("PCB")" has been inserted after the term "printed circuit board," on the second line of the paragraph. Accordingly, on the fifteenth line of the paragraph, the term "printed circuit board" has been replaced with "PCB." Also, on the seventeenth line, the term "respective" has been added before the term "cache" for clarification purposes.

In amended Figure 2, the reference numerals "4" and "6" have been removed in order to eliminate redundancy with previously used reference numerals.

In amended Figure 8, as requested by the Examiner, a passivation layer as described in paragraph [0034] of the specification has been added and labeled with reference numeral "50."

In amended Figure 12, as requested by the Examiner, a passivation layer as described in paragraph [0034] of the specification has been added and labeled with reference numeral "50."

In amended Figure 13, as requested by the Examiner, a passivation layer as described in paragraph [0034] of the specification has been added and labeled with reference numeral "50."

35 U.S.C. § 112 Claim Rejections

Claims 2, 3, 6, 8, 9, 11, 12, 20, 21, and 22 stand rejected under 35 U.S.C. § 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention. Applicant respectfully traverses this rejection, as hereinafter set forth.

In reference to claim 2, the examiner notes that it is unclear how the element "at least one trace" relates to independent claim 1. As a remedy, both claims 1 and 2 have been amended. Claim 1 originally included the elements "at least two signal traces" and "at least one voltage reference trace," but thereafter referred only to "the traces." To clarify claim 1, and in accordance with the language in the specification, the element of a "plurality of conductive traces" has been inserted to collectively refer to both "at least two signal traces" and "at least one voltage reference trace." In claim 2, corresponding language has been included. The old language of "at least one trace" has been replaced with "at least one of the plurality of conductive traces," in reference to independent claim 1.

Also in reference to claim 2, the examiner notes that the language "its length" is unclear. The examiner suggests replacing "its length" with "the length thereof." Accordingly, this change has been made.

In reference to claim 3, the examiner notes that the phrase "insulative layer" should follow "each." Accordingly, claim 3 now includes the phrase "each insulative layer."

In reference to claim 6, the examiner notes that it is unclear how the element "at least one of the conductive trace layers" relates to claim 1. As a remedy, both claims 1 and 2 have been amended. Claim 1 originally referred to "at least two conductive trace layers," and then later to "at least one of the at least two conductive trace layers." To clarify this language, and without changing the substance or scope of the claim, the element of "at least two conductive trace layers" has been replaced with a "plurality of conductive trace layers." The later reference in claim 1 follows as "at least one of the plurality of conductive trace layers." Accordingly, claim 6 has been modified to refer to "at least one of the plurality of conductive trace layers."

In reference to claim 8, the examiner notes that it is unclear how the element "at least one of the at least two conductive trace layers" relates to claim 1. In order to clarify this recitation, and to simplify the language of the entire claim, much of the language of claim 8 has been removed. The phrase "wherein at least one of the at least two conductive trace layers further comprises at least one voltage reference bus" has been removed. Accordingly, the identifier "the" after the phrase "is electrically coupled to" has been removed. These changes do not alter the scope or substance of claim 8, but merely simplify the language of claim 8.

In reference to claim 9, the examiner notes that it is unclear how the element "traces" is intended to be recited. The element "traces" of claim 9 refers collectively to the "at least two signal traces" and the "at least one voltage reference trace" of claim 1. As previously asserted herein, the language of claim 1 has been modified to include the element a "plurality of conductive traces," referring collectively to the "at least two signal traces" and the "at least one voltage reference trace." Accordingly, in claim 9, "the traces" has been modified to instead read "the plurality of conductive traces."

In reference to claim 11, the examiner notes that it is unclear whether the "at least one electrically conductive layer" may be properly characterized as being "comprised *in* the voltage reference portion" (Emphasis added). To clarify, the phrase "comprised in" has been replaced with the phrase "comprised of."

In reference to claim 12, the examiner notes that it is unclear whether "the voltage reference bus" and "traces extending therefrom" may properly depend from claim 10, which states that the voltage reference portion has "a greater surface area than the at least one signal trace." Claim 12 further defines and narrows the "voltage reference portion" of claim 10. Accordingly, the language of claim 12 has been modified to more clearly show the relationship between the elements of claim 12 and the "voltage reference portion" element of claim 10. In claim 13, the phrase "having" has been replaced with the phrase "with at least one." Additionally, the word "therefrom" was replaced with the more descriptive "from the voltage reference bus." Thus, the "voltage reference portion" of claim10 is further narrowed by claim 12 to comprise of

"a voltage reference bus with at least one voltage reference trace extending from the voltage reference bus."

In reference to claim 20, the examiner again notes that the element "traces" is unclear. The element "traces" was intended to refer collectively to the "at least two signal traces" and the "at least one voltage reference trace." To clarify this language, claim 20 has been modified to include the phrase "a plurality of conductive traces including" inserted just before the element "at least two signal traces." Thus, the element "a plurality of conductive traces" includes both the elements of "at least two signal traces" and "at least one voltage reference trace." Accordingly, the phrase "traces" has been modified to instead read "the plurality of conductive traces." Additionally, a "the" has been added after the phrase "such that," and "the at least" replaces the phrase "each of the," thus maintaining a proper antecedent basis.

Also in reference to claim 20, the examiner notes that it is unclear what characterizes "at least one component of the electronic system." The "at least one component" was intended to refer to at least one of the other elements of the electrical system outlined in claim 20. Accordingly, the phrase "at least one component of the electronic system" has been replaced with "at least one of the processor, the memory device, the at least one of an input device, the at least one of an output device, and the at least one of a data storage device."

In reference to claim 21, the examiner notes that the phrase "in its extent" is unnecessary and should be deleted. Accordingly, the phrase has been deleted from claim 21.

In reference to claim 22, the examiner notes that it is unclear what characterizes "at least one component of the electronic system." The components of the electrical system include those elements previously specified in the claim. To clarify this, the phrase "at least one component of the electronic system" has been replaced with "at least one of the processor, the memory device, the at least one of an input device, the at least one of an output device and the at least one of a data storage device."

35 U.S.C. § 102 Anticipation Rejections

Anticipation Rejection Based on U.S. Patent No. 6,040,524 to Kobayashi et al.

Claims 1 through 5, 7, 9, 10, 11, 15, 16, 18, and 19 stand rejected under 35 U.S.C. § 102(e) as being anticipated by Kobayashi et al. (U.S. Patent No. 6,040,524). Applicant respectfully traverses this rejection, as hereinafter set forth.

A claim is anticipated only if each and every element as set forth in the claim is found, either expressly or inherently described, in a single prior art reference. *Verdegaal Brothers v. Union Oil Co. of California*, 2 USPQ2d 1051, 1053 (Fed. Cir. 1987). The identical invention must be shown in as complete detail as is contained in the claim. *Richardson v. Suzuki Motor Co.*, 9 USPQ2d 1913, 1920 (Fed. Cir. 1989).

Kobayashi describes a printed circuit board comprising a dielectric lamina with two opposing surfaces (Col. 6, lines 42-49). On one of the surfaces is deposited a layer of microstrips constituting signal lines and ground areas, the ground areas arranged between the signal lines (Col. 6, lines 49-51, 61-63). On the other surface is a ground plane (Col 6, lines 54-55). Conductive means connect the ground plane to the ground areas interleaved with the signal lines (Col 7, lines 2-5). Implementation of the described printed circuit board arrangement onto multiple layer printed circuit boards is also taught (Col. 7, lines 26-63).

However, Kobayashi does not teach the spatial periodic coupling of a ground area or a voltage reference trace to a reference voltage at intervals predetermined to maintain a substantially consistent reference voltage throughout the ground area or voltage reference trace. As described in ¶ [0030] of the specification of the above-referenced application, periodic coupling of a reference trace is necessary to maintain a consistent voltage on the reference trace. In the absence of sufficient periodic coupling, the reference trace instead acts as an antenna. Thus, not only must the coupling to a reference voltage be periodic, the periodicity must also result in sufficiently dense coupling to avoid drifting of the reference trace voltage. The necessary density may be determined prior to the final manufacturing of the printed circuit board.

Because Kobayashi does not teach the sufficiently periodic coupling of a voltage reference trace to a reference voltage, and because this is taught in the specification of the above-

referenced application, claim 1 has been amended by requiring that "the at least one voltage reference trace [be] also spatially periodically coupled to a reference voltage at intervals predetermined to maintain a substantially consistent reference voltage throughout the at least one voltage reference trace." Therefore, it is respectfully submitted that Kobayashi does not anticipate each and every element of independent amended claim 1. Thus, under 35 U.S.C. § 102(e), independent amended claim 1 is allowable over Kobayashi.

Claims 2-5, 7 and 9 are each allowable, among other reasons, as depending either directly or indirectly from amended claim 1, which is allowable.

Independent claim 10 is directed to a printed circuit board comprising at least one electrically conductive layer which further includes a voltage reference portion and at least one signal trace. The voltage reference portion has a greater surface area than the at least one signal trace.

For the same reasons provided above with respect to independent claim 1, it is respectfully submitted that Kobayashi neither expressly nor inherently describes a printed circuit board that includes a voltage reference portion with at least one voltage reference trace spatially periodically coupled to a reference voltage. Accordingly, claim 10 has been amended to require that "the voltage reference portion comprises at least one voltage reference trace spatially periodically coupled to a reference voltage at intervals predetermined to maintain a substantially consistent reference voltage throughout the at least one voltage reference trace." Hence, Kobayashi does not anticipate each and every element of independent amended claim 10. Thus, under 35 U.S.C. § 102(e), independent amended claim 10 is allowable over Kobayashi.

Claim 11 is allowable, among other reasons, as depending either directly or indirectly from amended claim 10, which is allowable.

Independent claim 15 is directed to a printed circuit board that comprises at least one voltage reference plane substantially coextensive with a portion of a substrate.

For the same reasons provided above with respect to independent claim 1, it is respectfully submitted that Kobayashi neither expressly nor inherently describes a printed circuit board that includes a voltage reference plane spatially periodically coupled to a reference voltage. Accordingly, claim 15 has been amended to include "the voltage reference plane comprises at least one voltage reference trace spatially periodically coupled to a reference voltage at intervals predetermined to maintain a substantially consistent reference voltage throughout the at least one voltage reference trace." Hence, Kobayashi does not anticipate each and every element of independent amended claim 15. Thus, under 35 U.S.C. § 102(e), independent amended claim 15 is allowable over Kobayashi.

Claims 16 and 18 are allowable, among other reasons, as depending either directly or indirectly from amended claim 15, which is allowable.

Independent claim 19 is directed to a printed circuit board that comprises at least one voltage reference plane and a coplanar signal trace isolated therefrom.

For the same reasons provided above with respect to independent claim 1, it is respectfully submitted that Kobayashi neither expressly nor inherently describes a printed circuit board that includes a voltage reference plane spatially periodically coupled to a reference voltage. Accordingly, claim 19 has been amended to include "the voltage reference portion comprises at least one voltage reference trace spatially periodically coupled to a reference voltage at intervals predetermined to maintain a substantially consistent reference voltage throughout the at least one voltage reference trace." Hence, Kobayashi does not anticipate each and every element of independent amended claim 19. Thus, under 35 U.S.C. § 102(e), independent amended claim 19 is allowable over Kobayashi.

Anticipation Rejection Based on German Patent No. DD 239 899 A1

Claims 1, 3 through 5, 15, 16, 18, and 19 stand rejected under 35 U.S.C. § 102(b) as being anticipated by German Patent No. DD 239 899 A1 (hereinafter "the East German Patent"). Applicant respectfully traverses this rejection, as hereinafter set forth.

The East German reference describes a double-sided circuit board whereon pairs of signal lines and ground lines may be formed on either side of an insulating substrate. The widths of the ground lines are twice the widths of the corresponding signal lines. Ground lines are depicted in the accompanying figures as interleaved with the signal lines.

However, like Kobayashi, the East German patent does not teach the spatial periodic coupling of a voltage reference trace to a reference voltage at intervals predetermined to maintain a substantially consistent reference voltage throughout the extent of the voltage reference trace.

Because the East German patent does not teach the sufficiently periodic coupling of a voltage reference trace to a reference voltage, and because this is taught in the specification of the above-referenced application, claim 1 has been amended to include "the at least one voltage reference trace [be] also spatially periodically coupled to a reference voltage at intervals predetermined to maintain a substantially consistent reference voltage throughout the at least one voltage reference trace." Therefore, it is respectfully submitted that the East German patent does not anticipate each and every element of independent amended claim 1. Thus, under 35 U.S.C. § 102(b), independent amended claim 1 is allowable over the East German patent.

Claims 3, 4 and 5 are each allowable, among other reasons, as depending either directly or indirectly from amended claim 1, which is allowable.

Claim 5 is additionally allowable because the East German patent lacks any express or inherent description that the printed circuit board includes at least one voltage reference trace coupled to a voltage reference plane. Although Figure 4 of the East German patent depicts a voltage reference plane on one conductive layer of the substrate, it doesn't appear to Applicant that the voltage reference plane is coupled to the plurality of ground lines depicted on other

conductive layers. It is possible that the voltage reference plane holds a reference voltage other than that shared by the ground lines. Hence, it is not clear that the assumption that the depicted voltage reference plane and the ground lines are inherently coupled is a valid assumption.

Independent claim 15 is directed to a printed circuit board that comprises at least one voltage reference plane substantially coextensive with a portion of a substrate.

For the same reasons provided above with respect to independent claim 1, it is respectfully submitted that the East German patent neither expressly nor inherently describes a printed circuit board that includes a voltage reference plane spatially periodically coupled to a reference voltage. Accordingly, claim 15 has been amended to include "the voltage reference plane comprises at least one voltage reference trace spatially periodically coupled to a reference voltage at intervals predetermined to maintain a substantially consistent reference voltage throughout the at least one voltage reference trace." Hence, the East German patent does not anticipate each and every element of independent amended claim 15. Thus, under 35 U.S.C. § 102(b), independent amended claim 15 is allowable over the East German patent.

Claims 16 and 18 are allowable, among other reasons, as depending either directly or indirectly from amended claim 15, which is allowable.

Independent claim 19 is directed to a printed circuit board that comprises at least one voltage reference plane and a coplanar signal trace isolated therefrom.

For the same reasons provided above with respect to independent claim 1, it is respectfully submitted that the East German patent neither expressly nor inherently describes a printed circuit board that includes a voltage reference plane spatially periodically coupled to a reference voltage. Accordingly, claim 19 has been amended to include "the voltage reference portion comprises at least one voltage reference trace spatially periodically coupled to a reference voltage at intervals predetermined to maintain a substantially consistent reference voltage throughout the at least one voltage reference trace." Hence, the East German patent does not

anticipate each and every element of independent amended claim 19. Thus, under 35 U.S.C. § 102(b), independent amended claim 19 is allowable over the East German patent.

Anticipation Rejection Based on U.S. Patent No. 3,398,232 to Hoffman

Claims 1, 8, 9, and 13 stand rejected under 35 U.S.C. § 102(b) as being anticipated by Hoffman (U.S. Patent No. 3,398,232). Applicant respectfully traverses this rejection, as hereinafter set forth.

Hoffman describes a printed circuit board comprising a plurality of signal and reference traces interweaved together on at least two sides of a substrate. Col. 3, lines 17-35; Col. 4, lines 4-18. The reference traces are connected to a common reference bus. Col. 6, lines 16-24. Conducting plugs or vias connect signal traces or reference traces on opposing sides of the printed circuit board. Col. 4, lines 24-37.

However, Hoffman does not teach the spatial periodic coupling of a voltage reference trace to a reference voltage at intervals predetermined to maintain a substantially consistent reference voltage throughout the extent of the voltage reference trace. Consequently, because Hoffman does not teach the sufficiently periodic coupling of a voltage reference trace to a reference voltage, and because this is taught in the specification of the above-referenced application, claim 1 has been amended to include "the at least one voltage reference trace [be] also spatially periodically coupled to a reference voltage at intervals predetermined to maintain a substantially consistent reference voltage throughout the at least one voltage reference trace." Therefore, it is respectfully submitted that Hoffman does not anticipate each and every element of independent amended claim 1. Thus, under 35 U.S.C. § 102(b), independent amended claim 1 is allowable over Hoffman.

Claims 8 and 9 are each allowable, among other reasons, as depending either directly or indirectly from amended claim 1, which is allowable.

Independent claim 13 is directed to an electronic device that includes at least one voltage reference trace and at least two signal traces.

For the same reasons provided above with respect to independent claim 1, it is respectfully submitted that Hoffman neither expressly nor inherently describes an electronic device that includes a voltage reference trace spatially periodically coupled to a reference voltage. Accordingly, claim 13 has been amended to require that "the at least one voltage reference trace [is] spatially periodically coupled to a reference voltage at intervals predetermined to maintain a substantially consistent reference voltage throughout the at least one voltage reference trace." Hence, Hoffman does not anticipate each and every element of independent amended claim 13. Thus, under 35 U.S.C. § 102(b), independent amended claim 13 is allowable over Hoffman.

Anticipation Rejection Based on U.S. Patent No. 4,130,723 to Wakeling

Claims 1, 2, 10, 11, 15, 16, and 19 stand rejected under 35 U.S.C. § 102(b) as being anticipated by Wakeling (U.S. Patent No. 4,130,723). Applicant respectfully traverses this rejection, as hereinafter set forth.

Wakeling describes a printed circuit board comprising a double-sided insulated substrate with conductive trace layers on either or both sides. Col. 4, lines 15-32. Alternating signal tracks and ground tracks may be deposited on either side of the substrate. Col. 2, lines 9-11. Ground tracks further connect with a periphery track. Col. 2, lines 24-25. The ground tracks are wider than the signal tracks, and may comprise a majority of a conductive layer.

However, Wakeling does not teach the spatial periodic coupling of a voltage reference trace to a reference voltage at intervals predetermined to maintain a substantially consistent reference voltage throughout the extent of the voltage reference trace. Consequently, because Wakeling does not teach the sufficiently periodic coupling of a voltage reference trace to a reference voltage, and because this is taught in the specification of the above-referenced application, claim 1 has been amended to include "the at least one voltage reference trace [be] also spatially periodically coupled to a reference voltage at intervals predetermined to maintain a

substantially consistent reference voltage throughout the at least one voltage reference trace." Therefore, it is respectfully submitted that Wakeling does not anticipate each and every element of independent amended claim 1. Thus, under 5 U.S.C. § 102(b), independent amended claim 1 is allowable over Wakeling.

Claim 2 is allowable, among other reasons, as depending either directly or indirectly from amended claim 1, which is allowable.

Independent claim 10 is directed to a printed circuit board comprising at least one electrically conductive layer which further includes a voltage reference portion and at least one signal trace. The voltage reference portion has a greater surface area than the at least one signal trace.

For the same reasons provided above with respect to independent claim 1, it is respectfully submitted that Wakeling neither expressly nor inherently describes a printed circuit board that includes a voltage reference portion spatially periodically coupled to a reference voltage. Accordingly, claim 10 has been amended to include "the voltage reference portion comprises at least one voltage reference trace spatially periodically coupled to a reference voltage at intervals predetermined to maintain a substantially consistent reference voltage throughout the at least one voltage reference trace." Hence, Wakeling does not anticipate each and every element of independent amended claim 10. Thus, under 35 U.S.C. § 102(b), independent amended claim 10 is allowable over Wakeling.

Claim 11 is allowable, among other reasons, as depending either directly or indirectly from amended claim 10, which is allowable.

Independent claim 15 is directed to a printed circuit board that comprises at least one voltage reference plane substantially coextensive with a portion of a substrate.

For the same reasons provided above with respect to independent claim 1, it is respectfully submitted that Wakeling neither expressly nor inherently describes a printed circuit board that includes a voltage reference plane spatially periodically coupled to a reference voltage.

Accordingly, claim 15 has been amended to include "the voltage reference plane comprises at least one voltage reference trace spatially periodically coupled to a reference voltage at intervals predetermined to maintain a substantially consistent reference voltage throughout the at least one voltage reference trace." Hence, Wakeling does not anticipate each and every element of independent amended claim 15. Thus, under 35 U.S.C. § 102(b), independent amended claim 15 is allowable over Wakeling.

Claim 16 is allowable, among other reasons, as depending either directly or indirectly from amended claim 15, which is allowable.

Independent claim 19 is directed to a printed circuit board that comprises at least one voltage reference plane and a coplanar signal trace isolated therefrom.

For the same reasons provided above with respect to independent claim 1, it is respectfully submitted that Wakeling neither expressly nor inherently describes a printed circuit board that includes a voltage reference plane spatially periodically coupled to a reference voltage. Accordingly, claim 19 has been amended to include "the voltage reference portion comprises at least one voltage reference trace spatially periodically coupled to a reference voltage at intervals predetermined to maintain a substantially consistent reference voltage throughout the at least one voltage reference trace." Hence, Wakeling does not anticipate each and every element of independent amended claim 19. Thus, under 35 U.S.C. § 102(b), independent amended claim 19 is allowable over Wakeling.

In view of the foregoing, it is respectfully requested that the 35 U.S.C. §§ 102(b) and 102(e) rejections of claims 1-5, 7-11, 13, 15, 16, 18 and 19 be withdrawn.

35 U.S.C. § 103(a) Obviousness Rejections

Claims 6, 14, 17, 20, 21 and 22 stand rejected under 35 U.S.C. § 103.

M.P.E.P. 706.02(j) sets forth the standard for a Section 103(a) rejection:

> To establish a *prima facie* case of obviousness, three basic criteria must be met. First, there must be some suggestion or motivation, either in the references themselves or in the knowledge generally available to one of ordinary skill in the art, to modify the reference or combine reference teachings. Second, there must be a reasonable expectation of success. Finally, **the prior art reference (or references when combined) must teach or suggest all the claim limitations.** The teaching or suggestion to make the claimed combination and the reasonable expectation of success must both be found in the prior art, and not based on applicant's disclosure. *In re Vaeck*, 947 F.2d 488, 20 USPQ2d 1438 (Fed. Cir. 1991). (Emphasis added).

Obviousness Rejection Based on U.S. Patent No. 6,040,524 to Kobayashi et al or U.S. Patent No. 4,130,723 to Wakeling, in View of U.S. Patent No. 6,373,740 to Forbes et al.

Claims 6 and 17 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over Kobayashi et al. (U.S. Patent No. 6,040,524) or Wakeling (U.S. Patent No. 4,130,723), in view of Forbes et al. (U.S. Patent No. 6,373,740). Applicant respectfully traverses this rejection, as hereinafter set forth.

Claim 6 is allowable, among other reasons, as depending either directly or indirectly from claim 1, which is allowable. Claim 17 is allowable, among other reasons, as depending either directly or indirectly from claim 15, which is allowable.

Moreover, it is respectfully submitted that claims 6 and 17 are both allowable since the asserted combinations of Forbes with one of Kobayashi or Wakeling do not support a *prima facie* case of obviousness against either of these claims under 35 U.S.C. § 103(a).

In particular, one of ordinary skill in the art would not have been motivated to combine the teachings of Forbes with the teachings of either Kobayashi or Wakeling.

This is because Forbes does not provide one of ordinary skill in the art with any motivation to use a passivation layer whereon no further conductive layers will be deposited. Forbes teaches the use of an insulating layer on top of a conductive layer to facilitate deposition of an additional conductive layer. Col. 3, line 46 to Col. 4, line 31. As is well known in the art of printed circuit board design, vertical stacking of conductive traces is not possible without a

means for insulating each conductive trace layer from another. Deposition of an insulating layer between conductive layers is one such means. Application of insulation deposition means may be obvious to one skilled in the art *when an additional conductive layer is to be vertically stacked on top of existing conductive layers*. However, in the above-referenced application, additional vertical stacking is not anticipated, and hence, it would not be obvious to one skilled in the art to combine the teachings of Forbes with those of either Kobayashi or Wakeling.

As there is no motivational link between Forbes and either Kobayashi or Wakeling, it is respectfully submitted that any motivation to combine the teachings of Forbes with those of either Kobayashi or Wakeling could only have been improperly gleaned from the hindsight provided by the disclosure of the above-referenced application.

For these reasons, it is respectfully submitted that under 35 U.S.C. § 103(a), claims 6 and 17 are both allowable over the combination of Forbes with any of Kobayashi and Wakeling.

Obviousness Rejection Based on U.S. Patent No. 3,398,232 to Hoffman in View of U.S. Patent No. 6,373,740 to Forbes et al.

Claim 14 stands rejected under 35 U.S.C. § 103(a) as being unpatentable over Hoffman (U.S. Patent No. 3,398,232) in view of Forbes et al. (U.S. Patent No. 6,373,740). Applicant respectfully traverses this rejection, as hereinafter set forth.

Claim 14 is allowable, among other reasons, as depending either directly or indirectly from claim 13, which is allowable.

Moreover, it is respectfully submitted that claim 14 is allowable since the asserted combination of Forbes with Hoffman does not support a *prima facie* case of obviousness against this claim under 35 U.S.C. § 103(a).

In particular, one of ordinary skill in the art would not have been motivated to combine the teachings of Forbes with the teachings of Hoffman.

For the same reason provided above with respect to claims 6 and 17, one of ordinary skill in the art would not have been motivated to combine the teachings of Forbes with Hoffman in the manner that has been asserted. In particular, there would have been no motivation for one of

ordinary skill in the art, before the earliest priority date for the above-referenced application, to have used a passivation layer whereon no further conductive layers will be deposited. In the above-referenced application, additional vertical stacking is not anticipated, and hence, it would not be obvious to one skilled in the art to combine the teachings of Forbes with those of Hoffman.

Accordingly, it is respectfully submitted that, under 35 U.S.C. § 103(a), claim 14 is allowable over the combination of Forbes with Hoffman.

Obviousness Rejection Based on U.S. Patent No. 6,373,740 to Forbes et al. in View of U.S. Patent No. 6,040,524 to Kobayashi et al or U.S. Patent No. 4,130,723 to Wakeling

Claim 20 stands rejected under 35 U.S.C. § 103(a) as being unpatentable over Forbes et al. (U.S. Patent No. 6,373,740) in view of Kobayashi et al. (U.S. Patent No. 6,040,524) or Wakeling (U.S. Patent No. 4,130,723). Applicant respectfully traverses this rejection, as hereinafter set forth.

It is respectfully submitted that claim 20 is allowable since the asserted combinations of one of Kobayashi or Wakeling with Forbes does not support a *prima facie* case of obviousness against either of these claims under 35 U.S.C. § 103(a).

In particular, combining one of Kobayashi or Wakeling with Forbes does not teach or suggest all of the claim limitations of claim 20.

Neither Kobayashi nor Wakeling teach the spatial periodic coupling of a voltage reference trace to a reference voltage at intervals predetermined to maintain a substantially consistent reference voltage throughout the extent of the voltage reference trace. As described in the specification of the above-referenced application, periodic coupling of a reference trace is necessary to maintain a consistent voltage on the reference trace. In the absence of sufficient periodic coupling, the reference trace instead acts as an antenna. Thus, not only must the coupling to a reference voltage be periodic, the periodicity must also result in sufficiently dense coupling to avoid drifting of the reference trace voltage. The necessary density may be determined prior to the final manufacturing of the printed circuit board.

Because neither Kobayashi nor Wakeling teaches the sufficiently periodic coupling of a voltage reference trace to a reference voltage, and because this is taught in the specification of the above-referenced application, claim 20 has been amended to require that "the at least one voltage reference trace [be] also spatially periodically coupled to a reference voltage at intervals predetermined to maintain a substantially consistent reference voltage throughout the at least one voltage reference trace." Therefore, it is respectfully submitted that combining one of either Kobayashi or Wakeling with Forbes does not teach or suggest all of the claim limitations of claim 20. Thus, under 5 U.S.C. § 103(a), independent claim 20 is allowable over the combination of one of Kobayashi or Wakeling with Forbes.

Obviousness Rejection Based on U.S. Patent No. 6,373,740 to Forbes et al. in View of Either U.S. Patent No. 6,040,524 to Kobayashi et al or U.S. Patent No. 4,130,723 to Wakeling

Claim 21 stands rejected under 35 U.S.C. § 103(a) as being unpatentable over Forbes et al. (U.S. Patent No. 6,373,740) in view of either Kobayashi et al. (U.S. Patent No. 6,040,524) or Wakeling (U.S. Patent No. 4,130,723). Applicant respectfully traverses this rejection, as hereinafter set forth.

Claim 21 is allowable, among other reasons, as depending either directly or indirectly from claim 20, which is allowable.

Moreover, it is respectfully submitted that claim 21 is allowable since the asserted combination of one of Kobayashi or Wakeling with Forbes does not support a *prima facie* case of obviousness against this claim under 35 U.S.C. § 103(a).

In particular, combining one of Kobayashi or Wakeling with Forbes does not teach or suggest all of the claim limitations of claim 21.

For the same reason provided above with respect to claim 20, combining one of Kobayashi or Wakeling with Forbes does not teach or suggest the additional claim limitation added to claim 20. Accordingly, it is respectfully submitted that, under 35 U.S.C. § 103(a), claim 21 is allowable over the combination of one of Kobayashi or Wakeling with Forbes.

Obviousness Rejection Based on U.S. Patent No. 6,373,740 to Forbes et al. in View of Either U.S. Patent No. 4,130,723 to Wakeling or German Patent No. DD 239 899 A1

Claim 22 stands rejected under 35 U.S.C. § 103(a) as being unpatentable over Forbes et al. (U.S. Patent No. 6,373,740) in view of either Wakeling (U.S. Patent No. 4,130,723) or German Patent No. DD 239 899 A1. Applicant respectfully traverses this rejection, as hereinafter set forth.

It is respectfully submitted that claim 22 is allowable since the asserted combinations of one of Wakeling or the East German patent with Forbes does not support a *prima facie* case of obviousness against either of these claims under 35 U.S.C. § 103(a).

In particular, combining one of Wakeling or the East German patent with Forbes does not teach or suggest all of the claim limitations of claim 22.

Neither Wakeling nor the East German patent teach the spatial periodic coupling of a voltage reference trace to a reference voltage at intervals predetermined to maintain a substantially consistent reference voltage throughout the extent of the voltage reference trace.

Because neither Wakeling nor the East German patent teaches the sufficiently periodic coupling of a voltage reference trace to a reference voltage, and because this is taught in the specification of the above-referenced application, claim 22 has been amended by the additional phrase "and wherein the voltage reference plane comprises at least one voltage reference trace spatially periodically coupled to a reference voltage at intervals predetermined to maintain a substantially consistent reference voltage throughout the at least one voltage reference trace. Therefore, it is respectfully submitted that combining one of either Wakeling or the East German patent with Forbes does not teach or suggest all of the claim limitations of claim 22. Thus, under 5 U.S.C. § 103(a), independent claim 22 is allowable over the combination of one of Wakeling or the East German patent with Forbes.

For the foregoing reasons, withdrawal of the 35 U.S.C. § 103(a) rejections of claims 6, 14, 17 and 20-22 is respectfully requested.

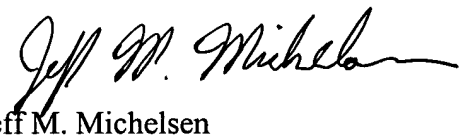
ENTRY OF AMENDMENTS

The amendments to claims 1-3, 6, 8-13, 15 and 19-22 above should be entered by the Examiner. New claim 23 should also be entered by the Examiner. The Examiner should enter these amendments and new claim because the amendments and new claim are supported by the as-filed specification and drawings and do not add any new matter to the application.

CONCLUSION

Claims 1-23 are believed to be in condition for allowance, and an early notice thereof is respectfully solicited. Should the Examiner determine that additional issues remain which might be resolved by a telephone conference, he is respectfully invited to contact Applicant's undersigned attorney.

Respectfully submitted,



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